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(54) Semiconductor device manufacture

(57) A method in which an isolating structure is defined by ion implantation in the presence of an attenuating windowed mask (1). The thickness of the mask e.g. oxide and the energy of the ions is chosen so that ions just penetrate the surface of a semiconductor substrate 3 underlying the mask 1 but deeply penetrate the substrate 3 in the region of the windows 5. Implantation is conducted at an elevated temperature so that amorphous material formation is prevented. This temperature may be reached and maintained by the heat of ion absorbtion, the substrate (1) being thermally isolated therefor.

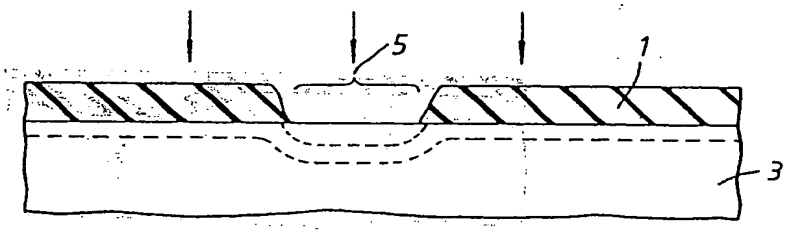

FIG. 1.

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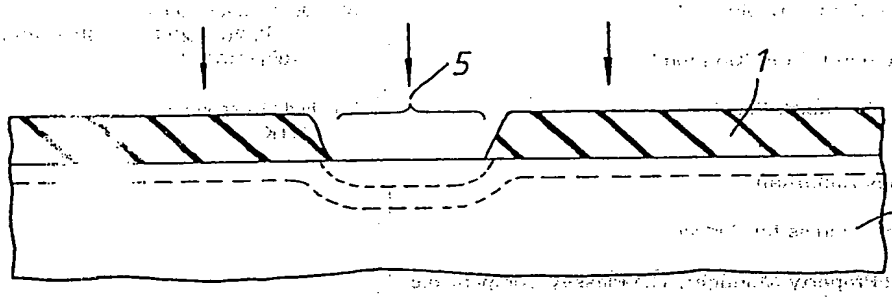

FIG. 1.

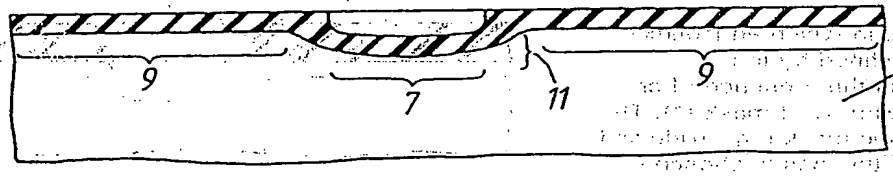

FIG. 2.

SPECIFICATION

Method of semiconductor device manufacture

Technical Field

The present invention concerns improvements in or relating to methods of semiconductor device manufacture, and in particular methods for producing devices having both lateral and vertical isolation structure.

Layers of dielectric material of lateral and vertical extent are employed to isolate regions of semiconductor material, providing thus insulation between adjacent elements of integrated circuits.

Background Art

Many techniques are known for depositing or forming dielectric layers. Surface implantation, as also selective area deep implantation, have been used to define lateral isolation layers. Following production of these layers, it is usual to adopt a masking layer to define active areas which are then produced by island etching or by LOCOS oxidation.

Disclosure of the Invention

The present invention provides an alternative method wherein lateral and vertical isolation layers are produced simultaneously, reducing thus the number of processing steps required during device manufacture.

In accordance with the invention there is thus provided a method of semiconductor device manufacture comprising the following steps:—providing, on the surface of a single crystal semiconductor material substrate, a windowed layer of energy absorbent material; implanting at an elevated temperature a relatively high dose of implant species at such a high energy sufficient to just penetrate the surface of the substrate underlying the windowed layer, and, to deeply penetrate the exposed semiconductor material; and, thereafter, annealing at a high temperature sufficient to consolidate dielectric material produced by reaction of the semiconductor material and the implanted species, forming lateral surface and buried layers and vertical layers.

In the aforesaid manner, lateral and vertical isolation structure is produced simultaneously. The depth of the buried lateral layer is dependent on the energy and dose of the implant radiation. The thickness of the energy absorbent layer is chosen according to the value of implant energy used and the depth to the buried layer.

Where silicon is chosen as the semiconductor material, it is convenient to adopt oxygen as the implant species to form thus layers of silicon oxide dielectric material. Other semiconductor materials (eg. gallium arsenide), and other implant species (eg. nitrogen) forming other dielectric materials (eg. silicon nitride) however, are not precluded from the general scope of this invention.

The substrate may be themally isolated, the energy of absorbtion elevating local temperature and maintaining the same. Alternatively, heaters may be used to assist in maintaining the substrate at the elevated temperature during implantation. This ensures that the semiconductor material, eg. silicon disturbed by implantation, recrystallises and does not form an amorphous structure.

In the foregoing definition the term vertical layers refers to layers providing continuity between the surface and buried lateral layers. No implication of strict verticality, therefore, is intended.

Brief Introduction of the Drawings

In the drawings accompanying this specification:—

Figures 1 and 2 are cross-sections of part of an integrated circuit illustrating implantation and dielectric layer formation performed by the method described herein.

Description of Preferred Embodiment

So that the invention may be better understood, an embodiment thereof will now be described with reference to the drawings. The description that follows is intended as example only.

As shown in Fig. 1 a covering layer 1 of energy absorbent material, in particular of silicon oxide, has been provided on the surface of a single crystal silicon semiconductor material substrate 3. This layer 1 may be so produced by either thermal growth or by conventional oxide deposition technique. Windows 5 have been opened in this covering layer 1 by means of a wet chemical etch—eg. buffered hydrofluoric acid etchant, following a step of photolithographic mask definition. It is noted that this wet etching results in the mask edge having a tapered profile. The resist mask has been removed by ashing and is not shown in Fig. 1.

This step of the process provides active area definition as is requisite for the integrated circuit device.

In the example illustrated, this step is followed by high energy, high dose implantation of oxidizing implant species—for example oxygen ions at an energy of 200keV and a dose of c. 2×10^{18} at/cm^2. At this high energy, full energy implantation into the silicon region exposed by the windows 5 results in the formation of a lateral layer 7 of buried silicon oxide dielectric material. Typically this layer 7 will be 4–5000Å thick and buried at a depth of 2–3000Å for the energy and dose stated. The thickness of the layer 1 of energy absorbent material,—eg. 2–3000Å oxide, that has been adopted, however, is such that the implant species penetrates only that silicon material that is near to the surface. At this sur-

face therefore a surface lateral layer 9 of dielectric material is produced. This layer 9 and the buried layer 7 are interconnected by a continuous "vertical" layer 11 lying beneath the window/mask interface 5/1. In this context it is noted that the depth of the buried layer 7 is comparable to the thickness of the surface layer 9. This avoids any discontinuity in the "vertical" layer 11 that extends between these lateral layers 7, 9. As the mask edge has a tapered profile, this also aids in producing layer continuity.

It is noted that the substrate is thermally insulated from its environment so that the silicon material, disturbed by implantation, will recrystalise at an elevated temperature (>350°C) reached and maintained by energy absorbed during implantation.

Following implantation, the substrate is annealed at a high temperature (>1150°C) to consolidate dielectric layer formation providing thus a more abrupt insulator/semiconductor interface, to anneal out implantation damage, and to smooth out any dopant redistribution.

Optionally, the covering layer 1 of oxide may be removed to facilitate further planar processing (Fig. 2).

Alternatively, it may be retained for reducing interconnect capacitance.

The method foregoing has, inter alia, application to VLSI silicon circuit processing (NMOS, CMOS).

It is also noted that the semiconductor material gallium arsenide will also react with implanted oxygen forming insulating dielectric material. With appropriate modification, the method foregoing, therefore, is also applicable to III–V semiconductor material processing.

CLAIMS

1. A method of semiconductor device manufacture comprising the following steps:—

providing, on the surface of a single crystal semiconductor material substrate, a windowed layer of energy absorbent material;

implanting at an elevated temperature a relatively high dose of implant species at such a high energy sufficient to just penetrate the surface of the substrate underlying the windowed layer, and, to deeply penetrate the exposed semiconductor material; and, thereafter,

annealing at a high temperature sufficient to consolidate dielectric material produced by reaction of the semiconductor material and the implanted species, forming lateral surface and buried layers and vertical layers.

2. A method as claimed in claim 1, wherein the substrate is thermally isolated such that it is raised to and maintained at the elevated temperature by implant energy absorbtion.

3. A method as claimed in claim 1 wherein one or more heaters are provided to maintain the substrate at the elevated temperature.

4. A method, as claimed in any one of the preceding claims wherein the energy absorbent material includes oxide.

5. A method, as claimed in any one of the preceding claims, wherein the implant species is oxygen.

6. A method of semiconductor device manufacture performed substantially as described hereinbefore with reference to and as shown in the accompanying drawings.

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